ABSTRACT

An automatic gain control RF signal processor for receiver systems, such as radar intercept receivers, includes an attenuator having an input for receiving an analog RF input signal, an amplifier coupled to the attenuator, a bandpass filter coupled to the amplifier output, a single ADC coupled to the bandpass filter, a digital logic circuit, and a FIFO buffer. The digital logic circuit has an input for receiving the ADC output signal, a first output coupled to a variable gain control input of the attenuator, and a second output. The logic circuit includes signal detection logic for detecting the presence of a pulse within the ADC signal, determining a peak amplitude value of the pulse, and based on the peak amplitude value generating an attenuation value at the first output that is applied to the variable gain control input of the attenuator. The sampling logic averages a number of ADC data samples to determine a moving average pulse amplitude, and compares this moving average pulse amplitude to a processing threshold value to determine a delta value with which to adjust an attenuation value for the attenuator, and to determine when to terminate a pulse and reset the attenuation value to zero. The averaging is carried out to determine whether an assigned number m of n samples is above the processing threshold value or whether the pulse should be terminated.